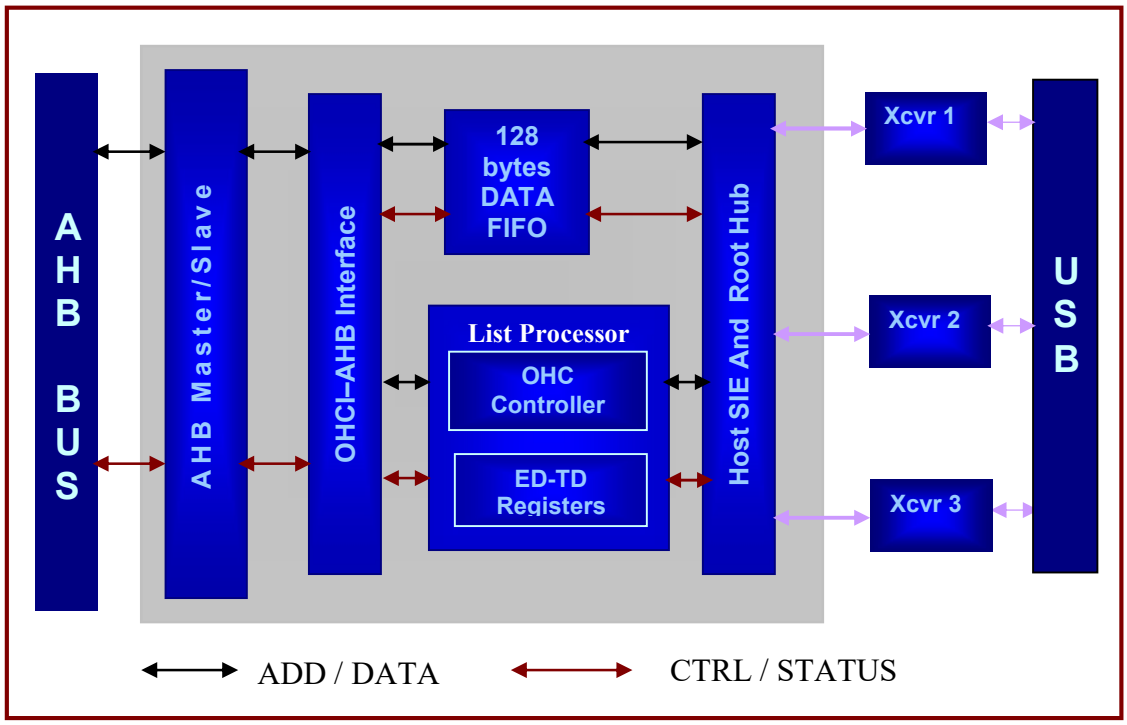
USB OPEN HOST CONTROLLER



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Overview

The silicon proven USB host controller from VinChip Systems is compliant with USB 1.1 and OHCI 1.0 Specifications. The core is designed for flexibility and ease of use and facilitates implementation of a wide variety of applications with fast turnaround time. This core is technology independent and migrating it to any technology is fast and simple. This OHC can be easily interfaced to standard buses such as Motorola, ARM, S-Bus, etc.,

Key Features

- Silicon proven.
- USB Specification 1.1 compliant
- 33 MHZ AHB 2.1 compliant
- VHDL / Verilog source code provided
- Supports low and full speed devices

- Technology independent
- Integrated root hub with 3 ports
- Supports 127 devices
- Bridging core to other system buses like ARM, Motorola, Sun, etc.,
- Supports Control, Bulk, Isochronous and Interrupt data transfer types.

Description

The USB OHCI Core comprises the following blocks.

AHB Master Slave Function

The AHB Master/Slave function is a bus interface unit that performs all data transfers necessary for the back-end OHC Core to access the system-memory as well as the data transfers necessary for the bus master to access the AHB bus. The target functionality supports memory read/write and configuration read/write commands. The tasks of master function are

- Fetching Endpoint Descriptors (Eds) and Transfer Descriptors (TDs)
- Read/Write Endpoint data from/to system memory.
- Accessing HC Communication Area (HCCA)
- Write Status and Retire TDs. .

OHC-AHB Interface

This block acts as the interface between the OHC Controller block and AHB master/slave. It controls data flow among AHB function, data buffer and ED-TD registers. All the OHC specific operational registers except for the root hub reside in this block.

List processor block

This block implements the USB Operational States of the Host Controller as defined in the OHCI Specification. It also generates SOF tokens every 1ms and triggers the List Processor while HC is in the Operational State. This block processes the lists scheduled by HCD according to the priority set in the operational registers.

Data FIFO

This block contains a 64 * 8 FIFO to store the data returned by Endpoints on IN transactions and the data to be sent to the Endpoints on OUT transactions.

Root Hub

The Root Hub is integrated into the host controller and it consists of the hub repeater which handles

- Connectivity setup and tear down.
- Exception handling (babble, loss of activity)
- Connect / disconnect detection.

Host SIE

This is the Bus protocol manager. It handles the following.

- Serial to parallel conversion and vice-versa.
- CRC generation and checking
- NRZI encoding / decoding

Products & Services

VinChip's array of USB products include device cores for various peripherals like Mice, Keyboards, Joysticks, Monitors, Speakers, Printers, Scanners and UPS. These soft cores come with comprehensive documentation, verification environment, test suite and tech support. We also undertake device driver development. Our core maintenance program includes updates and corrections. Please contact us at info@vinchip.com for more information on our products and services.