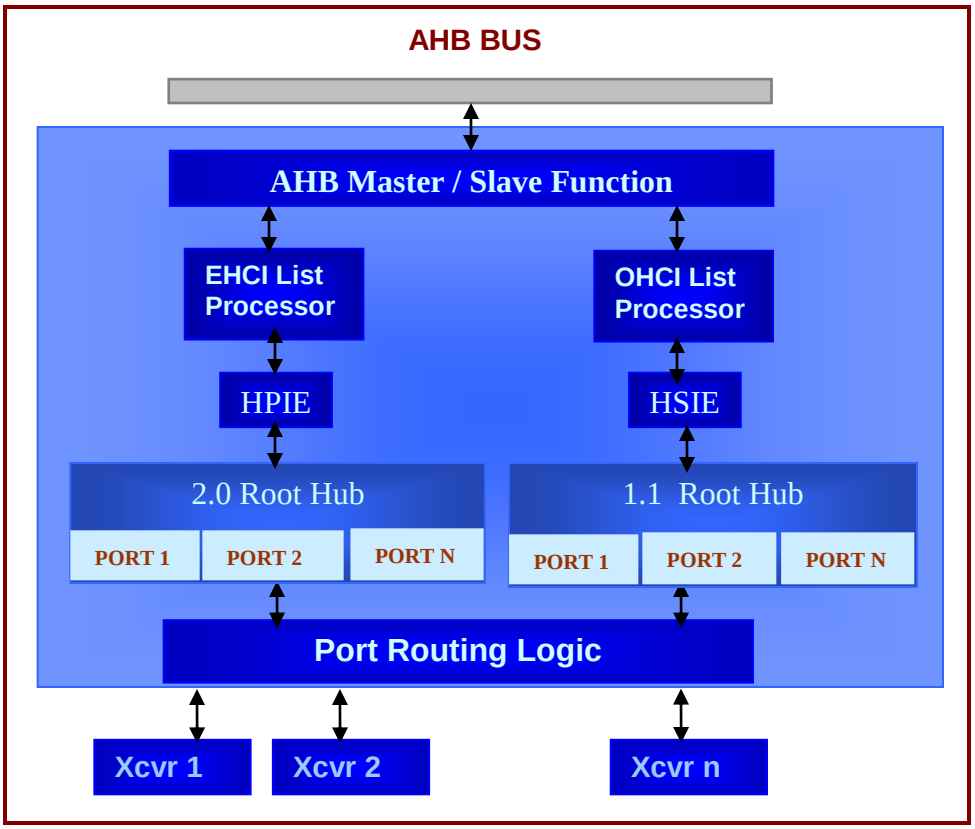
EHCI / OHCI USB 2.0 Host Controller Core



Overview

VinChip's USB 2.0 Host controller is designed for flexibility and ease of use and facilitates implementation of a wide variety of applications with fast turnaround time. This design is technology independent and migrating it to any technology is fast and simple. This EHC can be easily interfaced to standard buses such as ARM, S-Bus, etc.,

Key Features

- VHDL / Verilog source code provided
- USB EHCI specification compliant
- 33 MHZ AHB 2.1 compliant
- Supports low, full and high speed devices
- Technology independent
- Integrated root hub with upto 8 ports

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- Supports 127 devices
- Bridging the core to other system buses like ARM, Motorola, Sun, etc.,
- Supports Control, Bulk, Isochronous and interrupt data transfer types

Description

The EHCI Core comprises the following blocks.

AHB Master Slave Function

The AHB Master/Slave function is a bus interface unit that performs all data transfers necessary for the back-end core to access the system memory as well as the data transfers necessary for the bus master to access the AHB BUS. The target functionality supports memory read/write and configuration read/write commands. It has two functions. Function zero corresponds to USB 1.1 Host controller and Function two to USB 2.0 Host controller.

The master supports memory read and memory write burst and single data phase transactions. The main functions are reading and writing EHCI specific data structures and data transfer from the system memory to the device and vice-versa.

EHCI LIST PROCESSOR

This block takes care of the USB transaction with high speed devices, which are USB 2.0 compliant. It processes the EHCI ver 2.0 specific data structures.

OHCI LIST PROCESSOR

This block takes care of the USB transaction with full and low speed devices, which are specification 1.1 compliant. This block only processes USB 1.1 compliant data structures.

HPIE

This parallel interface engine decodes the packet from the device and also does CRC checking

HSIE

This is the host serial interface engine for USB 1.1 OHCI List processor engine. It does NRZI encoding / decoding, bitstuffing / debitstuffing, CRC checking / generation, packet decoding and serial to parallel conversions and vice versa.

USB 2.0 Root Hub

This block takes care of USB 2.0 device specific connect/disconnect, power management, suspend and resume signaling.

USB 1.1 Root Hub

This block takes care of USB 1.1. device specific connect/disconnect, power management, suspend and resume signaling.

Port Routing Logic

Depending on device speed this block switches different downstream devices to either USB 2.0 or USB 1.1 root hubs.

Products & Services

VinChip's suite of soft cores for SoCs includes USB, AHB, Bluetooth and Infiniband controllers. These soft cores come with comprehensive documentation, verification environment, test suite, drivers and tech support. Please contact us at the address given below for more information on our products and services.