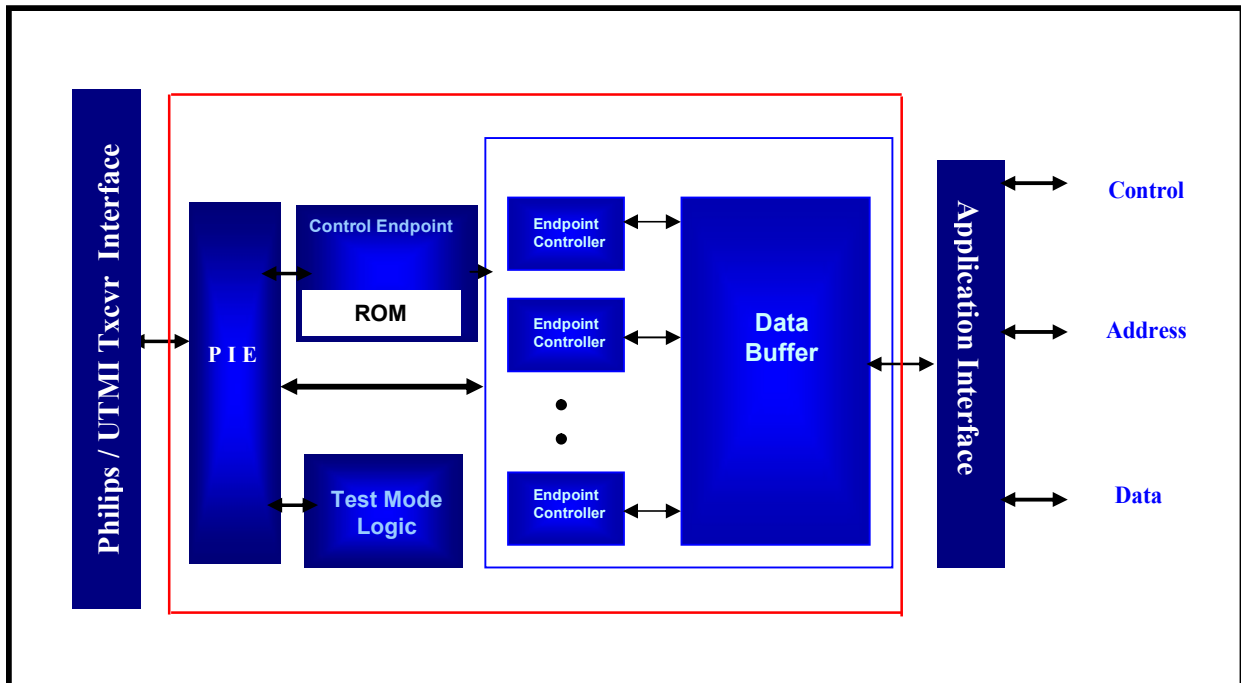


## USB 2.0 Device Core



**VinChip Systems**

Vinchip systems, Inc  
 6020 Muldrow Rd,  
 Carmichael, CA 95608,  
 Ph: (408) 777-2922  
 Email: info@vinchip.com  
 www.vinchip.com



## Overview

VinChip's USB 2.0 soft core facilitates data transmission up to 480 Mbps and is ideally suited for high-speed devices like CD-Rom drives, Video camera etc. This document describes its salient features and internal organization.

## Key Features

- USB 2.0 compliant
- Technology and Process independent
- Supports both UTMI and Philips transceivers
- Remote Wakeup Feature Support
- Control, Bulk, Interrupt and Isochronous transfer support
- Endpoint FIFOs are internal to the device

- Parametrizable endpoint features for number, transfer type, direction of transfer, maximum packet size
- Dual port RAM used for FIFO implementation
- Supports all standard requests
- Vendor specific request supported
- Utility for wiring endpoints and generating descriptors
- AHB interface support

## Description

### PIE (Parallel Interface Engine)

PIE acts as a bridge between the control, non-control endpoints and the transceiver. It gets the 16-bit raw data from the transceiver and splits and segregates the PID, CRC, data payload bits and delivers to the appropriate endpoints. It checks all the basic USB protocol needs viz. PID, CRC, time-out etc., during reception and packetizes the data-payload with proper PID and CRC bits, during transmission. It also handles the high-speed detection handshake protocol, suspend and resume signaling etc.

### Control Endpoint

This block handles all the 3-stages (setup, data and status) of control transfers. It checks validity of device requests using a LUT. Descriptor information of the device is stored in a ROM housed inside the control endpoint. Address decoder also resides in this block.

### Non-Control Endpoint

Non-Control endpoints include endpoints supporting interrupt, bulk and isochronous data transfers. Each endpoint has an endpoint controller and a FIFO. The endpoint controller manages the USB transaction protocol, data-handling

of the FIFO, and maintains integrity of the data. The FIFO residing in the endpoint is the data storage area. Up to 30 high-speed endpoints with different transfer types could be configured based on the need.

## TEST-MODE

This block handles the test-mode operation of the device-controller. It supports the following test modes: Test\_SE0\_NAK, Test\_J, Test\_k and Test\_Packet. A ROM housed inside the test-mode logic stores the test-packet to be transmitted for Testmode Test Packet command.

## Application Interface

Application interface block provides a seamless interface to popular processor buses. Variants are available to support VCI. Supports DMA transfer type.

## Products & Services

VinChip's suite of soft cores for SoCs includes USB, PCI, Bluetooth and Infiniband controllers. These soft cores come with comprehensive documentation, verification environment, test suite, Drivers and tech support. Please contact us at [info@vinchip.com](mailto:info@vinchip.com) for more information on our products and services.

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