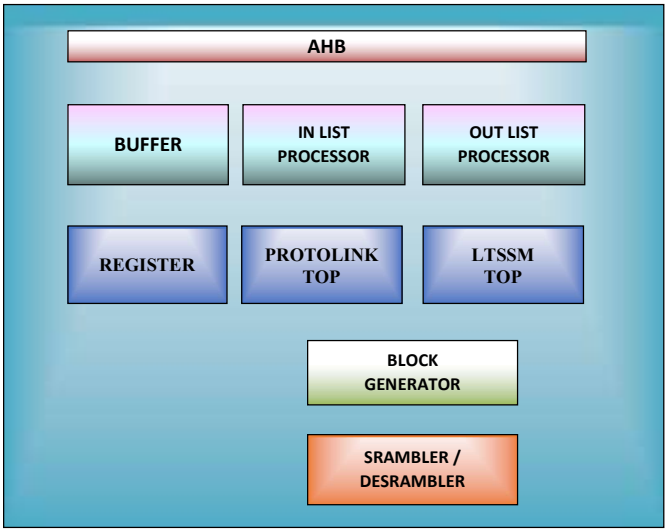

USB3.2 SuperSpeed Plus Device

The Super Speed Plus USB bus is implemented as a separate dual simplex dual lane data path consisting of two uni-directional differential links, one for transferring data from the host to Device3.2 and one for transferring data from Device3.2 to the USB host. The D+/D- signal pins defined by USB 2.0 are not used for Super Speed Plus operation but are provided to allow for backward compatible operation.

The Vinchip VUSB3.2DC core provides a USB functional device controller that conforms to the USB 3.2 specification for Super-Speed Plus (20Gbps, 10Gbps, 5Gbps, 480 and 12 Mbps) functions. The core is user-configurable for up to 15 IN Endpoints and up to 15 OUT Endpoints in addition to Endpoint 0 (EP0). These additional Endpoints can be individually programmed for bulk/interrupt or isochronous transfers. Each Endpoint requires an associated FIFO. The VUSB3.2DC has a RAM interface for connecting to a single block of synchronous dual-port RAM. The FIFO for Endpoint 0 is fixed at 512 bytes. The other Endpoint FIFOs may range upto the Maximum packet size of bytes in size and can buffer 1 or more packets. Separate FIFOs may be associated with each Endpoint.

The VUSB3.2DC provides a USB 3.2 Transceiver Interface (UTMI extension to usb3.2) to connect to an Super-Speed Plus transceiver. Access to the FIFOs and internal control/status registers may be via a 32-bit AMBA AHB-compatible synchronous CPU interface via the AMBA AHB bridge. The VUSB3.2DC has a RAM interface for connecting to the single block of synchronous RAM that is used for all the Endpoint FIFOs. The device also offers support for DMA access to the Endpoint FIFOs. (The VUSB3.2DC-AHB bridge includes DMA controller hooks.)

Major product features:

- Complies with USB 3.2 standard for Super Speed Plus(20Gbps, 10Gbps and 5.0 Gbps), Hi-Speed (480 Mbps) and Full-Speed (12 Mbps) Backward compatible with usb2.0 and the type C connectors.
- Technology and Process independent
- Data Interface is dual simplex dual lane data path consisting of two uni-directional differential links, separate from USB2.0 signaling.
- Supports Super speed UTMI transceiver interface with extension to the existing UTMI
- Interface for USB2.0 Configurable up to 15 additional IN or OUT Endpoints
- Compatible USB transfer support for Control, Bulk, Interrupt and Isochronous transfers using USB3.2 Transaction/Handshake Packets and the Data Packets.
- Bus Transaction protocol is host directed and has asynchronous traffic flow. The packet traffic is explicitly routed.
- Parametrizable endpoint features for number, transfer type, direction of transfer, maximum packet size
- Built-in 32-bit synchronous AMBA AHB compatible CPU interface
- Support for DMA access to FIFOs
- Synchronous Dual Port RAM interface for FIFOs
- Supports suspend and resume signaling
- Fully synthesizable
- Support all standard, Vendor specific control transfer requests Utility for core configuration of device descriptors and to wire endpoints.

This Super-Speed Plus function controller provides the entire USB
packet of encoding, decoding, and checking interrupting the CPU only when the Endpoint data has been successfully transferred. An Utility is provided for configuring the core to the user's requirements. This document describes its salient features and its internal organization below

USB2.0 Device controller
This block contains the PIE (parallel interface engine), control endpoint and the non control endpoint controller blocks of the usb2.0 device. It interfaces to the backend bus through the endpoint RAM blocks and the device configuration registers.

PIE interface between the usb2.0 utmi phy interface and the device logical function endpoints. Control Endpoint handles all the control transfers of the usb2.0 device including enumeration, standard and
vendor specific requests. Non control Endpoint controller handles bulk, ISO and interrupts transfer for the Backend application.

USB3.2 Device controller blocks
This block contains the SSPPIE (Super Speed Plus PHY Interface Engine, usb3.2 super speed plus control endpoint, usb3.2 super speed plus non-control endpoint blocks. In interfaces with the backend application through the USB3.2 Configuration Register set and the Endpoint RAM interface.

SSPPIE interfaces between the usb3.2 super speed plus signals of the UTMI transceiver extension

Control Endpoint handles all the control transfers of the usb2.0 device including enumeration, standard
and vendor specific requests.

Non control Endpoint controller handles bulk, ISO and interrupt transfer for the Backend application.

RAM Interface
The RAM controller provides an interface to a dual-port synchronous RAM of size 16Kb, which is used to buffer packets between the MCU and the USB.

Application Bus Interface
Application interface block provides a seamless interface to popular processor buses. Variants are available to support 32-bit AMBA AHB compatible CPU, PCI and VCI.

Supports DMA transfer type.