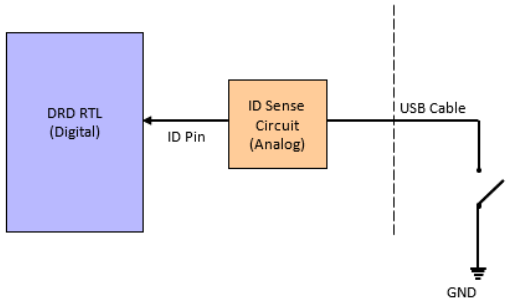
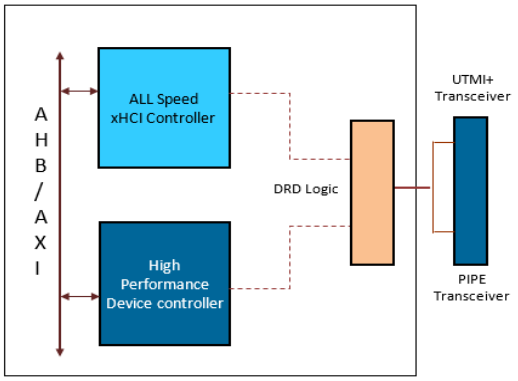




DRD Controller

Introduction

DRD is a supplement to the USB3.0 specification where a USB host and a USB device are integrated into a single USB port (i.e.) one transceiver/PHY. The user has the benefit to connect their hand gadgets to a PC or to a keyboard, mouse, pen drive etc (ie) the DRD can connect to a USB host or a device.

Vinchip device controller and xHCI host controller are two independent digital blocks on AHB or AXI and are integrated together to make the DRD.

xHCI with all speed support

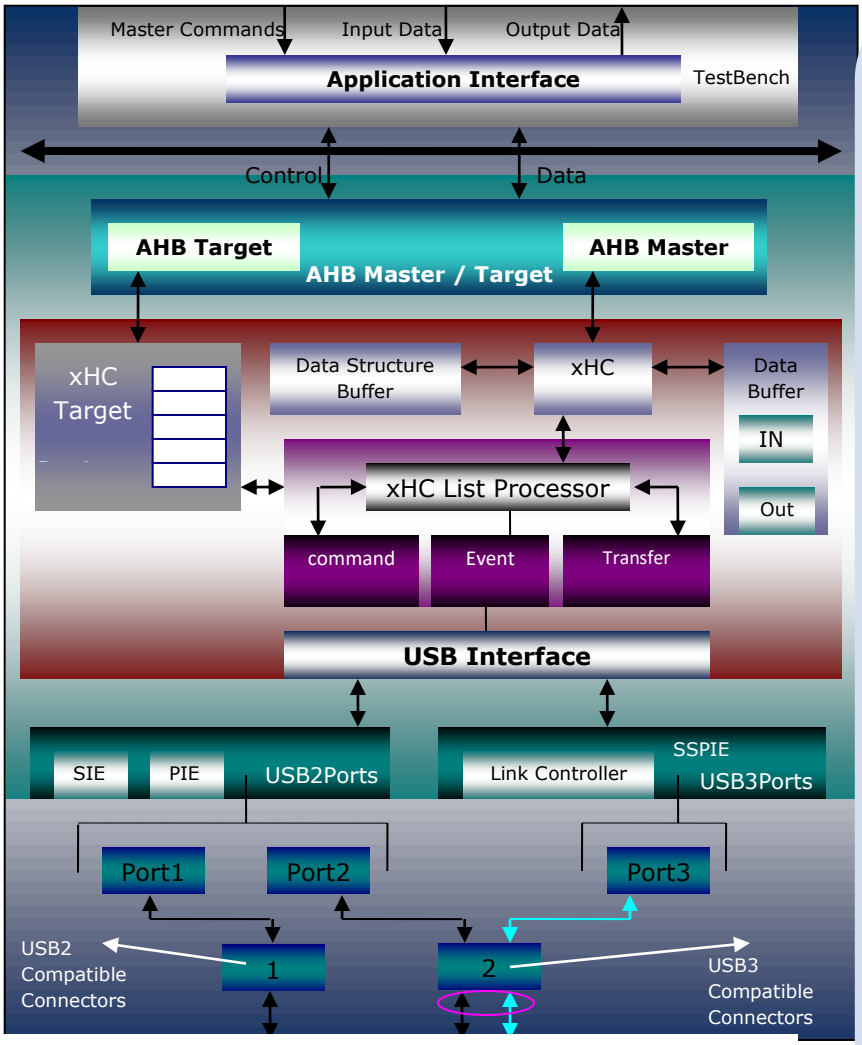
When acting as a Host our DRD controller supports all USB devices through the Linux USB stack. Linux USB stack supports audio, video, modem, printer etc.

Our xHCI host controller has been tested with Windows and Android operating systems and since xHCI is a standard specification for USB host controllers, it should work in any other operating system.

USB 3 Device with all speed support

When connected to a host controller, our DRD works as a USB device. We provide sample firmware for Mass storage. We also support UDC Linux driver.

In addition, we can provide our RISC V CPU as part of the IP.



USB3.0 Super-Speed Host

The Vinchip Super-Speed USB Host Controller is designed for flexibility, ease of use and provides ASIC/FPGA designers to implement a complete USB3.0 Host for 5 Gbps operation. The Host packet traffic can be explicitly routed and need not be broadcasted. The VUSB30xHC can be customized and optimized as a standalone host chip or integrated into ASIC for a variety of applications such as PCs, Smart phone's, etc. The D+/D- signal pins defined by USB 2.0 are not used for Super Speed operation but are provided to allow for backward compatible operation. The design is technology independent and can be easily processed in most technologies. It can be easily bridged to any industry standard bus including the PCI, PCI Express and AMBA AHB, AXI interfaces.

Super-Speed USB3.0 Extensible Host Controller (VUSB30xHCI)

The Vinchip VUSB30xHC core provides a USB functional host controller that conforms to the USB 3.0 specification for Super-Speed (5 Gbps, 480 Mbps, 12 Mbps and 1.5 Mbps) functions. The xHC Host Controller has the flexibility to support USB2.0 and USB3.0 thus eliminating the need for the companion Host Controllers. It supports USB3.0 Power Management Enhancements and also enables USB Resource Management across VMs.

The extensible Host controller utilizes a common Host Buffer to initiate an USB Bus transaction for both Super-speed and USB2.0 devices. The RAM is used all kinds of USB transfers. The Bus interface unit handles the TRB transfer data storage with the ost buffers only through Bus Master DMA data transfers.

Major product features

- Complies with USB 3.0 Standard for Super Speed (5 Gbps), High Speed (480 Mbps), Full-Speed (12 Mbps) and Low-Speed (1.5 Mbps).
- Complies with Intel xHCI specification for USB (revision 0.9).
- 32-bit and 64-bit addressing capability.
- Backward compatible with USB2.0 Devices and the type A connectors.
- Eliminates the need for companion host controllers along with its associated host software.
- Supports Bulk Streaming protocol and Data bursting.
- Supports Super speed USB PIPE and UTMI+ or ULPI transceiver interface.
- Supports USB3.0 Hub with simultaneous USB3.0 and 2.0 device transfers through the same hub. Also supports USB2.0 ping and USB2.0 Hub split transactions.
- Synchronous dual port scalable 2K RAM buffer separately for IN and OUT transfers.
- Compatible USB transfer support for Control, Bulk, Interrupt and Isochronous transfers using USB3.0 Transaction / Handshake Packets and the Data Packets.
- Technology and Process independent.
- Built-in 32-bit synchronous AMBA AHB-compatible CPU interface
- Integrated Root Hub and expandable downstream ports with support for all the USB bus speeds.
- Supports USB3.0 Power Management enhancements with suspend and resume.
- Fully synthesizable
- Utility for generation of ports expandability for the Host's downstream port.

Deliverables

- Verilog source code and test-bench.
- Scripts for Simulation and key features

VinChip's USB 2.0 Host controller is designed for flexibility and ease of use and facilitates implementation of a wide variety of applications with fast turnaround time. This design is technology independent and migrating it to any technology is fast and simple. This EHC can be easily interfaced to standard buses such as ARM, S-Bus, etcocumentation and Application Notes.

The VUSB30xHCI provides a USB 3.0 Host PIPE and UTMI+ or ULPI Transceiver Interface to connect to a Super-Speed USB transceiver. The AMBA AHB target interface provides access to the xHC internal control/status registers for a 32-bit AMBA AHB-compatible synchronous CPU through the AHB- bus bridge.

The VUSB30xHCI handles data transfers to/from the RAM (host buffers) through AHB Bus Master (DMA access) to transfer TRB data between the System Memory (Application software). The Vinchip xHCI Host controller for USB3.0 utilizes the host memory based transaction schedules.

This Super-Speed host controller provides the entire USB packet of encoding / decoding and also initiating Transaction packets (TP) and Data Packets (includes Data Packet Header (DPH) and Data Packet (DP)) through command TRBs, and notifies the host software with the USB events through event TRBs. USB3.0 also supports bulk streaming and burst transfers with sequence of ordered data packets, which can also recover the error packets during transfers.

A Utility is provided for parameterizing the downstream ports of the host core to the user's requirements.

This document describes its salient features and its internal organization below.

USB3.0 Host PHY Interface and Root Hub

This block contains the SSDPIE (Superspeed Downstream PHY interface engine), HPIE (host parallel interface engine), HSIE (host serial Interface engine) and its root hub to handle the USB Devices. It interfaces to the xHC list processor through the USB interface block. The root hub block controls the USB downstream ports and also reports the port status information to the host software through the xHCI registers.

SSDPIE interfaces with the USB3.0 super speed signals of the USB3.0 PIPE transceiver interface.

HPIE interfaces between the USB2.0 UTMI+ PHY interface and the xHCI Host Controller block.

HSIE interfaces between the USB1.1 serial interface of the UTMI+ transceiver and the xHCI Host Controller block.

- **Root Hub** handles downstream USB device connectivity, USB evVHDL / Verilog source code provided
- USB EHCI specification compliant
  - 33 MHZ AHB 2.1 compliant
  - Supports low, full and high speed devices
  - Technology independent
  - Integrated root hub with upto 8 ports

USB3.0 Extensible Host controller blocks

This block contains the xHCI list processor which handles command TRB handling to initiate USB transactions, event TRBs to notify asynchronous information and transaction responses to the host software. The Transfer TRBs provide data source/sink for the data transfers to/from the USB devices.

USB3.0 xHCI List Processor handles all the processing of the command TRBs, to initiate transactions, handshake and data packets on the USB3.0 device including link layer management. It handles transaction responses and all USB asynchronous notifications to the host software through event TRBs. It also provides enhanced link power management support.

USB3.0 xHCI Register Set, Data structure and Data Buffers are responsible for controlling the USB host controller, providing status information and providing storage of host scheduled structures and USB data to handles USB transaction with the devices.

RAM Interface

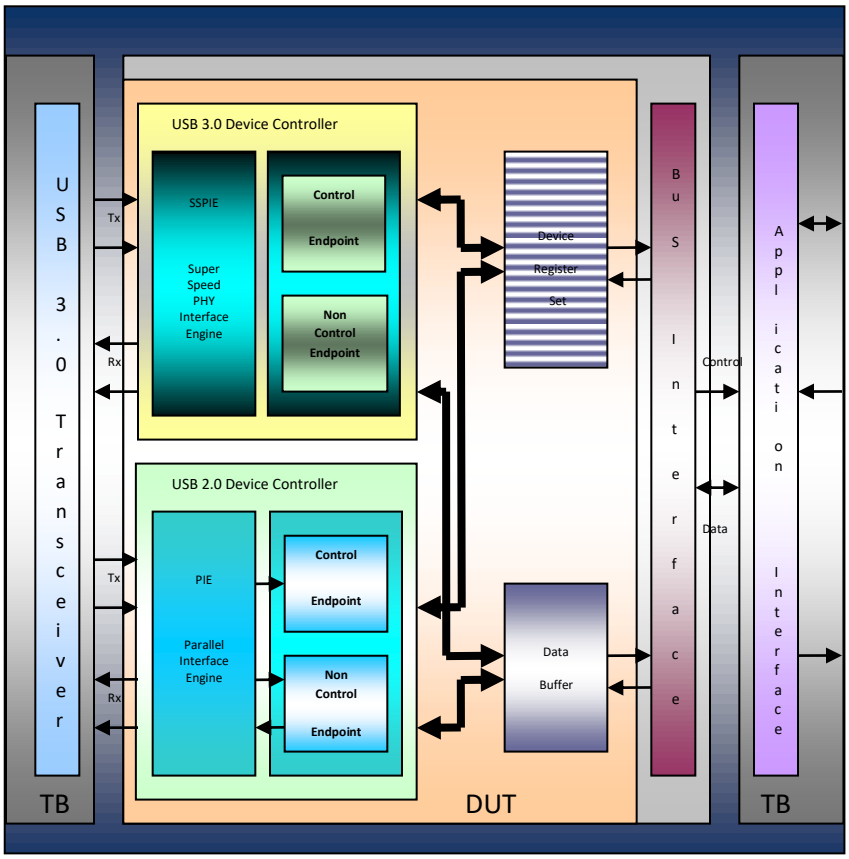
The RAM controller provides an interface to a dual-port synchronous RAM of size 4Kb, which is used to buffer packets between the MCU and the USB. Separate IN and OUT RAM buffer of each 2K is provided for the USB data transfers.

Application Bus Interface

Application interface block provides a seamless interface to popular processor buses. Variants are available to support 32-bit AMBA AHB compatible CPU, PCI, PCI Express and VCI. Also, support DMA type of transfer.

Products & Services

VinChip's suite of soft cores for SoCs includes USB, WUSB, WiMedia Mboa Mac, PCI, AHB2PCI, SATA, Ethernet, PCI_Express and Bluetooth controllers. These soft cores come with comprehensive documentation, verification environment, test suite, Drivers and tech support. Please contact us at info@vinchip.com for more information on our products and services.



USB3.0 Superspeed Device

The Super Speed USB bus is implemented as a separate dual-simplex data path consisting of two uni-directional differential links, one for transferring data from the host downstream to peripherals and one for transferring data from peripherals upstream to the host. The D+/D- signal pins defined by USB 2.0 are not used for Super Speed operation but are provided to allow for backward compatible operation.

Super-Speed USB Device Controller (VUSB30DC)

The Vinchip VUSB30DC core provides a USB functional Device controller that conforms to the USB 3.0 specification for Super-Speed (5Gbps, 480 and 12 Mbps) functions. The core is user-configurable for up to 15 IN Endpoints and up to 15 OUT Endpoints in addition to Endpoint 0 (EP0). These additional Endpoints can be individually programmed for bulk/interrupt or isochronous transfers.

Each Endpoint requires an associated FIFO. The VUSB30DC has a RAM interface for connecting to a single block of synchronous dual-port RAM. The FIFO for Endpoint 0 is fixed at 64 bytes. The other Endpoint FIFOs may range upto the Maximum packet size of bytes in size and can buffer 1 or more packets. Separate FIFOs may be associated with each Endpoint.

Major product features

- Complies with USB 3.0 standard for Super Speed(5.0 Gbps), Hi-Speed (480 Mbps) and Full-Speed (12 Mbps)
- Backward compatible with usb2.0 and the type A connectors.
- Technology and Process independent
- Data Interface is Dual-simplex, 4-wire differential signaling, separate from USB2.0 signaling.
- Supports Super speed UTMI transceiver interface with extension to the existing UTMI Interface for USB2.0
- Configurable up to 15 additional IN or OUT Endpoints
- Configurable FIFO sizes from 8 to 16K with option of dynamic FIFO sizing
- Compatible USB transfer support for Control, Bulk, Interrupt and Isochronous transfers using USB3.0 Transaction/Handshake Packets and the Data Packets.
- Bus Transaction protocol is host directed and has asynchronous traffic flow. The packet traffic is explicitly routed.
- Parametrizable endpoint features for number, transfer type, direction of transfer, maximum packet size and FIFO size
- Built-in 32-bit synchronous AMBA AHB-compatible CPU interface
- Support for DMA access to FIFOs
- Synchronous Dual Port RAM interface for FIFOs
- Supports suspend and resume signaling
- Fully synthesizable
- Support all standard, Vendor specific control transfer requests
- Utility for core configuration of device descriptors and to wire endpoints.

Deliverables

- Verilog source code and test-bench
- scripts for simulation and synthesis

The VUSB30DC provides a USB 3.0 Transceiver Interface (UTMI extension to usb3.0) to connect to an Super-Speed transceiver. Access to the FIFOs and internal control/status registers may be via a 32-bit AMBA AHB-compatible synchronous CPU interface via the AMBA AHB Bridge.

The VUSB30DC has a RAM interface for connecting to the single block of synchronous RAM that is used for all the Endpoint FIFOs. The device also offers support for DMA access to the Endpoint FIFOs. (The VUSB30DC-AHB Bridge includes DMA controller hooks.)

This Super-Speed function controller provides the entire USB packet of encoding, decoding, and checking interrupting the CPU only when the Endpoint data has been successfully transferred.

An Utility is provided for configuring the core to the user's requirements.

This document describes its salient features and its internal organization below.

USB2.0 Device controller
This block contains the PIE (parallel interface engine), control endpoint and the non control endpoint controller blocks of the usb2.0 device. It interfaces to the backend bus through the endpoint RAM blocks and the device configuration registers.

PIE interface between the usb2.0 utmi phy interface and the device logical function endpoints.

Control Endpoint handles all the control transfers of the usb2.0 device including enumeration, standard and vendor specific requests.

Non control Endpoint controller handles bulk, ISO and interrupt transfer for the Backend application.

USB3.0 Device controller blocks
This block contains the SSPIE (Super Speed PHY Interface Engine, usb3 super speed control endpoint, usb3 super speed non-control endpoint blocks. In interfaces with the backend application through the USB3.0 Configuration Register set and the Endpoint RAM interface.

SSPIE interfaces between the usb3.0 super speed signals of the UTMI transceiver extension

Control Endpoint handles all the control transfers of the usb2.0 device including enumeration, standard and vendor specific requests.

Non control Endpoint controller handles bulk, ISO and interrupt transfer for the Backend application .

RAM Interface
The RAM controller provides an interface to a dual-port synchronous RAM of size 16Kb, which is used to buffer packets between the MCU and the USB.

Application Bus Interface

Application interface block provides a seamless interface to popular processor buses. Variants are available to support 32-bit AMBA AHB compatible CPU, PCI and VCI. Supports DMA transfer type.

Products & Services

VinChip's suite of soft cores for SoCs includes USB, WUSB, WiMedia Mboa Mac, PCI, AHB2PCI, SATA, Ethernet, PCI_Express and Bluetooth controllers. These soft cores come with comprehensive documentation, verification environment, test suite, Drivers and tech support. Please contact us at info@vinchip.com for more information on our products and services.

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