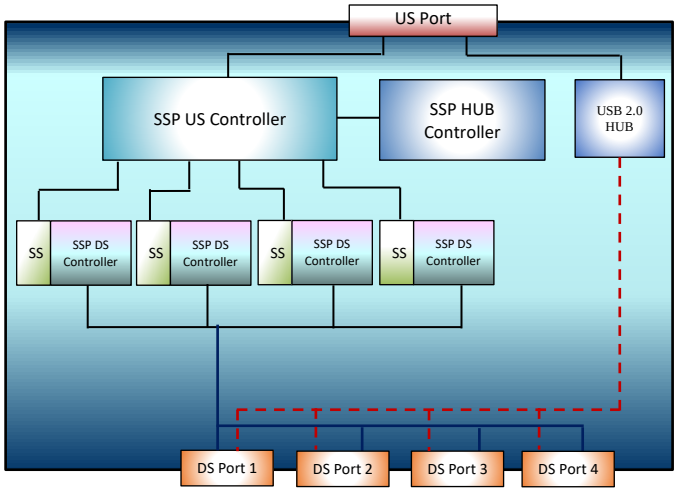

USB3.2 SuperSpeed Hub

The Super Speed Plus USB bus is implemented as a separate dual-simplex dual lane data path consisting of two uni-directional differential links, one for transferring data from the host downstream to Hub3.2 or USB3.2 Peripherals and one for transferring data from Hub or Peripherals upstream to the USB host.
The D+/D- signal pins defined by USB 2.0 are not used for Super Speed Plus operation but are provided to allow for backward compatible operation.

Super-SpeedPlus USB3.2 Hub Controller (VUSB3.2 HUB)

The Vinchip VUSB3.2 HUB core provides a USB3.2 functional SSP US Controller, SSP Hub controller and SSP DS Controller that conforms to the USB 3.2 specification for Enhanced Super-Speed (with four different rates gen2x2 -20Gbps , gen2x1 - 10Gbps , gen1x2 - 10Gbps and gen1x1 - 5 Gbps)and with backward compatible USB2.0 Hub (480, 12 and 1.5 Mbps) functions. The 3.2 Hub Repeater / Forwarder is responsible for connectivity setup, tear down, bus fault detection and recovery and connect / disconnect detection. Hub specific status and control commands allows host to configure the hub and control its individual downstream facing ports. The backward compatible USB 2.0 Hub core consists of Hub Controller, Repeater and Transaction Translator.

The VUSB3.2 HUB provides a USB 3.2 Transceiver Interface (UTMI extension to usb3.2) to connect to a super speed Plus transceiver.

Major product features:

- Supports two lanes or one lane - easily configurable
- Number of downstream ports can be easily selected
- Complies with USB 3.2 standard for Super-Speed Plus (10 Gbps), Super-Speed (5.0 Gbps), Hi-Speed (480 Mbps), Full-Speed (12 Mbps) and Low-Speed (1.5 Mbps).
- Backward compatible with USB2.0 devices and hubs and the type A connectors.
- Technology and Process independent.
- Data Interface is Dual-simplex, 4-wire differential signaling for each lane, separate from USB2.0 signaling with downstream connect / disconnect detection.
- Supports Super speed UTMI transceiver interface with extension to the existing UTMI Interface for USB2.0
- Super-Speed plus Hub3.2 consists of Hub Forwarder/Repeater and a Hub Controller.
- Separate Header Buffers for each Upstream and Downstream Port's traffic Forwarding / Repeating.
- Compatible USB transfer support for Control and Interrupt transfers to USB3.2 Hub using USB3.2 Transaction / Handshake Packets and the Data Packets.
- Super-speed Plus Independent Data Packet Buffering and Concurrent transactions in both Upstream and Downstream directions
- Bus Transaction protocol is host directed and has asynchronous traffic flow. The packet traffic is explicitly routed.
- Store and Forward more than one data packets at the same time.
- End-to-End Protocol will retry for recovery.
- Support all standard and Hub specific control transfer requests.
- Super-speed plus Repeater / Forwarder reclock packets in both the directions.
- Supports suspend and resume signaling and also handle Hub Power Management.
- Utility for wiring of parameterizable downstream Ports, its routing and descriptor generation.
- Fully synthesizable.

Deliverables:

- Verilog source code and test-bench.
- Scripts for simulation and synthesis.

The VUSB32HUB has a USB2.0 Hub and a Super-Speed plus Hub comprising of the USB3.2 Hub controller and the Hub Repeater / Forwarder. The Hub Repeater/Forwarder is responsible for managing connectivity between upstream and downstream facing ports which are operating at Super Speed Plus or SuperSpeed. The USB 3.2 Architecture allows concurrent transactions to occur in both the upstream and downstream directions.

This document describes its salient features and its internal organization below.

USB2.0 Hub controller
This block consists of the Hub Controller, Repeater and Transaction Translator. The Hub Controller provides the mechanism for host to hub communication. Hub-specific status and control commands permit the host to configure a hub and to monitor and control its transaction translator and individual downstream ports.

Hub Controller - PIE interface between the usb2.0 utmi phy interface and the hub controller containing a control endpoint and a status change endpoint. The **Control Endpoint** handles all Hub2.0 specific requests. The **Status Change Endpoint** reports the Hub and its Downstream Port Status to the upstream USB Host.

Transaction Translator handles all the usb transfers between the High speed USB2.0 Host/Hub on the upstream with the USB1.1 legacy devices.

Hub Repeater (High / Full Speed) handles either broadcasting of the upstream packets on the downstream or repeating any one of the downstream packets to the upstream.

USB3.2 Hub controller and Forwarder/Repeater

The Super Speed Plus hub portion consists of three functional components: the Super Speed Plus Upstream Controller, the Super Speed plus Downstream Controller and the Super Speed plus Hub Controller.

The Super Speed plus Upstream (SSP US) Controller is responsible for the behavior of the upstream port, buffering for packets being received from the upstream link, buffering and arbitrating packets waiting to be transmitted on the upstream link, and for routing packets to the appropriate downstream port's Downstream Controller (or to the hub controller).

The Super Speed plus Downstream (SSP DS) Controller is responsible for the behavior of the downstream port, buffering for packets being received from the downstream link, buffering and arbitrating packets waiting to be transmitted on the downstream link and for routing Packets to the Upstream Controller.

The Super Speed plus Hub Controller provides the same mechanism for host-to-hub communication that the SuperSpeed Hub Controller does.

The Hub Controller provides status and control and permits host access to the Super Speed plus Hub. A Utility is provided for configuring the hub downstream ports to the user's requirements.

VUSB3.2 HUB SuperSpeedPlus Store and Forward Behavior

The SuperSpeedPlus Hub has the following general functionality.

In the downstream direction:

Receives and validates packet
Forwards packet to appropriate downstream port
Selects next packet to transmit on (each) downstream port

In the upstream direction:

Receives and validates packet
Forwards packet to the upstream port
Selects next packet to transmit on the upstream port

Products & Services

VinChip's suite of soft cores for SoCs includes USB, PCI, AHB2PCI, SATA, Ethernet, PCI_Express, Wireless and Bluetooth controllers. These soft cores come with comprehensive documentation, verification environment, test suite, Drivers and tech support. Please contact us at info@vinchip.com for more information on our products and services.